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09/632,759	08/04/2000	Richard J. Selvaggi	ATI-000118BN	2358

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EXAMINER	
AMINI, JAVID A	
ART UNIT	**PAPER NUMBER**
2672	5

DATE MAILED: 07/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/632,759	SELVAGGI ET AL.	
	Examiner	Art Unit	
	Javid A Amini	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☒ Claim(s) 1-18 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicant's arguments filed on May 09, 2003 have been fully considered but they are not persuasive.

- The corrected or substitute drawings were received on May 09, 2003. These drawings are acceptable.
- Response to remarks on page 11, regarding 35 U.S.C. 112: the rejection of claims 1, 5, 11 and 17 under 35 USC 112 are withdrawn.
- Response to remarks on page 12, second paragraph: Applicant discloses that the image data is including: position data, color data, and texture data. Examiner interpretation: texture data comprises of color data. Applicant should be able to show the equations that determine the position, texture and color data in this invention.
- Response to remarks on page 13, regarding 35 U.S.C. 102(b): Applicant in line 3 discloses that the reference does not separate the image data by the arithmetic operation. In contrast, Ashburn in (col. 10, lines 9-67) and (col. 11, lines 1-43) discloses an equation that calculates parameters for each pixel (examiner's interpretation: the position data are known on X and Y coordinates for each pixel, and the color data are calculated with respect to intensity of color of red/blue/green along X and Y axis). Therefore, according to the above interpretation the reference Ashburn encloses the applicant's invention regarding image data.

- Applicant on page 14 of remarks discloses about Ashburn system that if all the equations for the first triangle have not been completed, it would not be possible to achieve the efficiencies desired. The reference in Fig. 1, illustrates the processor and frame buffer board and geometry accelerator chips 32A, 32B and 32C increase the system bandwidth for this purpose mentioned above.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-18 rejected under 35 U.S.C. 102(b) as being anticipated by Ashburn U.S. patent 5,651,106, dated July 22, 1997.

1. Claim 1.

"A method for processing video image data including a plurality of different image data types, the method comprising the steps of: providing tasks to be performed on each different image data type of data; dividing the image data into a plurality of groups based on the image data type, determining a set of arithmetic operations required to accomplish the tasks provided for the corresponding image data type; assigning each arithmetic operation to one of a plurality of commonly used arithmetic units; performing each arithmetic operation by the assigned

arithmetic unit whereby each image data type is transformed in accordance with the corresponding provided tasks; and combining the transformed image data of each group". Ashburn in Figs. 12 and 16 illustrates plurality of data groups, which are representing vertex parameters. Ashburn divides the image data into groups with known addresses based on positions (position of vertex V0...2 shown by X,Y and Z) and colors (colors of vertex V0...2 shown by R,G and B; also textures are part of color pixel) in Fig. 16. Ashburn discloses in Fig. 3 that is a block diagram of exemplary circuit elements for performing plane equation generation. ALU (Arithmetic Logic Unit) 184, Multiplier 186, and Divider 188 are operatively connected to a Register File 180 and a RAM (Random Access Memory) 196 through a multiplexer/data formatter 182. Performing and assigning an arithmetic unit is inherent because in processing of video image data an arithmetic assigned to perform color manipulation of pixels in certain area and also the certain area can be divide to smaller areas (vertex) and more arithmetic can be assigned to that area. One process of arithmetic provide position of data and the other process will provide the content of pixel data and another arithmetic cab be assigned to perform the depth of the pixel. Ashburn discloses in Fig. 3 the options of Addition and Subtraction, Multiplication and Division. Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R,G,B color control signals for each pixel are respectively provided over R,G,B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive.

2. Claim 2.

"The method of claim 1 wherein the plurality of image data groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". See rejection of claim 1.

3. Claim 3.

"The method of claim 1 wherein the plurality of said commonly used arithmetic units includes an addition unit and a multiplication unit". See rejection of claim 1.

4. Claim 4.

"The method of claim 1 wherein the determining step is based on in part by a sequence of arithmetic state". See rejection of claim 1.

5. Claim 5.

"The method of claim 1 further comprising the step of providing a queue for each of the plurality of commonly used arithmetic units wherein each assigned arithmetic operation is sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is inherent because providing a queue or generating

plane equation for particular task or following a procedure required to assign an arithmetic operation.

6. Claim 6.

"The method of claim 5, wherein each task includes one or more steps of one or more arithmetic operation types such that the steps of a task can be performed by different arithmetic units, the steps to be performed in a sequence, the method further comprising the step of preventing the arithmetic units from performing the arithmetic operations of a task out of sequence". This step is inherent because if the design of a task is correct, the arithmetic operations will follow the sequence, otherwise it operates out of sequence.

7. Claim 7.

"An apparatus for processing video image data including a plurality of different image data types, the apparatus comprising: means for providing tasks to be performed on each different image data type; means for dividing the image data into a plurality of groups based on the image data type; means for determining a set of arithmetic operations required to accomplish the tasks provided for the corresponding image data type; means for assigning each arithmetic operation to one of a plurality of commonly used arithmetic units; means for performing each arithmetic operation by the assigned arithmetic unit whereby each image data type is transformed in accordance with the corresponding provided tasks; and means for combining the transformed image data of each group". Ashburn in Figs. 12 and 16 illustrates plurality of data groups, which are representing vertex parameters. Ashburn divides the image data into groups

with known addresses based on positions (position of vertex V0...2 shown by X,Y and Z) and colors (colors of vertex V0...2 shown by R,G and B; also textures are part of color pixel) in Fig. 16. Ashburn discloses in Fig. 3 that is a block diagram of exemplary circuit elements for performing plane equation generation. ALU (Arithmetic Logic Unit) 184, Multiplier 186, and Divider 188 are operatively connected to a Register File 180 and a RAM (Random Access Memory) 196 through a multiplexer/data formatter 182. Performing and assigning an arithmetic unit is inherent because in processing of video image data an arithmetic assigned to perform color manipulation of pixels in certain area and also the certain area can be divide to smaller areas (vertex) and more arithmetic can be assigned to that area. One process of arithmetic provide position of data and the other process will provide the content of pixel data and another arithmetic cab be assigned to perform the depth of the pixel. Ashburn discloses in Fig. 3 the options of Addition and Subtraction, Multiplication and Division. Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R,G,B color control signals for each pixel are respectively provided over R,G,B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive.

8. Claim 8.

"The apparatus of claim 7 wherein the plurality of image data groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". See rejection of claim 7.

9. Claim 9.

"The apparatus of claim 7 wherein the plurality of said commonly a used arithmetic unit includes an addition unit and a multiplication unit". See rejection of claim 7.

10. Claim 10.

"The apparatus of claim 7 wherein for each image data group, the arithmetic operation set includes a set of arithmetic states and the determined operations for each task are defined by a sequence of the set's arithmetic states". See rejection of claim 7.

11. Claim 11.

"The apparatus of claim 10 further comprising a queue for each of said commonly used arithmetic units and wherein each arithmetic operation is sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is inherent because providing a queue or generating plane equation for particular task or following a procedure required to assign an arithmetic operation.

12. Claim 12.

"The apparatus of claim 11 further comprising means for preventing the arithmetic units from performing the arithmetic operations of a task out of sequence". This step is inherent because if the design of a task is correct the arithmetic operations will follow the sequence, otherwise it operates out of sequence.

13. Claim 13.

"An apparatus for performing video processing, the video processing including performing tasks on vertex parameters, the apparatus comprising a scheduler having an input configured to receive tasks, said scheduler arranging the vertex parameters to be processed into a plurality of groups based on in part characteristics of the vertex parameters; a sequencer for each group, said sequencer: determining the tasks required to process that group's parameters, determining a set of arithmetic operations required to accomplish that group's tasks, assigning each arithmetic operation to be performed to one of a plurality of commonly used arithmetic units, and sending each of the arithmetic operations of each of that group's tasks to the arithmetic unit associated with that arithmetic operation; and each of said commonly used arithmetic units, having an input configured to receive the sent arithmetic operations and vertex parameters associated with the sent operations, each arithmetic unit performing the sent arithmetic operations on the sent vertex parameters". Ashburn in Figs. 12 and 16 illustrates plurality of data groups, which are representing vertex parameters. Ashburn divides the image data into groups with known addresses based on positions (position of vertex V0...2 shown by X,Y and Z) and colors (colors of vertex V0...2 shown by R,G and B; also textures are part of color pixel) in Fig. 16. Ashburn discloses in Fig. 3 that is a block diagram of exemplary circuit elements for performing plane

equation generation. ALU (Arithmetic Logic Unit) 184, Multiplier 186, and Divider 188 are operatively connected to a Register File 180 and a RAM (Random Access Memory) 196 through a multiplexer/data formatter 182. Performing and assigning an arithmetic unit is inherent because in processing of video image data an arithmetic assigned to perform color manipulation of pixels in certain area and also the certain area can be divide to smaller areas (vertex) and more arithmetic can be assigned to that area. One process of arithmetic provide position of data and the other process will provide the content of pixel data and another arithmetic cab be assigned to perform the depth of the pixel. Ashburn discloses in Fig. 3 the options of Addition and Subtraction, Multiplication and Division. Ashburn discloses in (col. 4, lines 52-63) the frame buffer board then combines, on a pixel by pixel basis, the object color values with the resultant texture data provided from the texture mapping board, to generate resulting image R,G,B values for each pixel. R,G,B color control signals for each pixel are respectively provided over R,G,B lines 29 to control the pixels of the display screen to display a resulting image on the display screen that represents the texture mapped primitive.

14. Claim 14.

"The apparatus of claim 13 wherein the plurality of groups includes a position group for position vertex parameters, a color group for color vertex parameters and a texture group for texture vertex parameters". Ashburn illustrates in Fig. 1A that the distributor chip 30 receives the X,Y,Z coordinate and color primitive data over bus 16 from the host computer, and distributes 3-D primitive data evenly among the 3-D geometry accelerator chips 32A, 32B and 32C. The texture

mapping data transfers over bus 94. In this manner, the system bandwidth is increased because three groups of primitives are operated upon simultaneously.

15. Claim 15.

"The apparatus of claim 13 wherein said plurality of said commonly a used arithmetic unit includes an addition unit and a multiplication unit". See rejection of claim 13.

16. Claim 16.

"The apparatus of claim 13 wherein for each group, the arithmetic operation set includes a set of arithmetic states and the determined operations for each task are defined by a sequence of the set's arithmetic states". See rejection of claim 13.

17. Claim 17.

"The apparatus of claim 16 further comprising a queue for each of said commonly used arithmetic units and wherein the sent arithmetic operations are sent to the queue associated with its commonly used arithmetic unit". Ashburn discloses in (col. 2, lines 22-67; col. 3, lines 1-15) that the invention is directed to a computer graphic system apparatus for generating pixel data representative of a triangle, comprising a processing circuit for generating plane equation data in response to vertex data representative of a triangle, and a fill scan converter responsive to the processing circuit of the plane equation data for generating pixel data representative of the triangle. Also the step is inherent because providing a queue or generating plane equation for particular task or following a procedure required to assign an arithmetic operation.

18. Claim 18.

"The apparatus of claim 17 wherein said sequencer prevents said arithmetic units from performing the arithmetic operations of a task out of sequence". This step is inherent because if the design of a task is correct the arithmetic operations will follow the sequence, otherwise it operates out of sequence.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Javid A Amini whose telephone number is 703-605-4248. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-8705 for regular communications and 703-746-8705 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-0377.

Javid Amini
July 11, 2003

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600